I CLAIM:

1. Apparatus for processing data, said apparatus comprising:

an instruction decoder responsive to program instructions to control data processing operations; and

an address offset generating circuit controlled by said instruction decoder and operable to generate an N-bit address offset having a value specified by an address offset generating instruction including an offset value sign specifying bit S; wherein

said N-bit address offset has bit values B_i when expressed as a two's complement number, where $(N-1)\geq i\geq Z$ and $(N-1)>Z\geq 0$, said address offset generating instruction includes L high order field bits P_k, where $(N-Z)>L\geq 1$ and $L>k\geq 0$, and said address offset generating circuit is operable such that:

(i) if all of said high order field bits P_k have respective predetermined values D_k, then bits B_j of said N-bit address offset are given by $B_j = S$ for all values of j such that $(N-1)\geq j\geq(N-L-1)$; and

(ii) if any of said high order field bits P_k does not have said predetermined value D_k, then bits B_j of said N-bit address offset, where $(N-1)\geq j\geq(N-L-1)$, are given by a predetermined one-to-one mapping from combinations of values of said high order field bits P_k and said offset value sign specifying bit S to combinations of values of B_j other than the combination $B_j = 1$ for all values of j such that $(N-1)\geq j\geq(N-L-1)$ and the combination $B_j = 0$ for all values of j such that $(N-1)\geq j\geq(N-L-1)$.

2. Apparatus as claimed in claim 1, wherein said predetermined values D_k are all equal to 1.

3. Apparatus as claimed in claim 1, wherein said address offset generating circuit is operable to generate bit B_j values of said N-bit address offset each bit value B_j having a value given by a respective predetermined one of:

$B_j = S$ for one directly sign bit specified value of j;

$B_j = S \text{ XOR } P_{k(j)} \text{ XOR } D_{k(j)}$ where k(j) is a one-to-one index mapping from values of j, excluding said directly sign bit specified value of j, to values of k.

4. Apparatus as claimed in claim 3, wherein said directly sign bit specified value of j is N-1.

5. Apparatus as claimed in claim 1, wherein said address offset generating instruction is a branch instruction and said N-bit address offset is an N-bit branch target address offset.

6. Apparatus as claimed in claim 5, wherein said N-bit branch target address offset is combined with a program address of said branch instruction to generate a branch target address.

7. Apparatus as claimed in claim 1, wherein said N-bit address offset is further sign extended by said address offset generating instruction prior to use.

8. Apparatus as claimed in claim 1, wherein L = 2.

9. Apparatus as claimed in claim 1, wherein N = 25.

10. Apparatus as claimed in claim 1, wherein Z is one of 1 and 2.

11. Apparatus as claimed in claim 1, wherein bit values B_{N-2-L} to B_Z are directly specified in said address offset generating instruction.

12. A method of processing data, said method comprising the steps of:

controlling data processing operations using an instruction decoder responsive to program instructions; and

generating an N-bit address offset having a value specified by an address offset generating instruction including an offset value sign specifying bit S using an address offset generating circuit controlled by said instruction decoder; wherein

said N-bit address offset has bit values B_i when expressed as a two's complement number, where $(N-1) \geq i \geq Z$ and $(N-1) > Z \geq 0$, said address offset generating instruction includes L high order field bits P_k, where $(N-Z) > L \geq 1$ and $L > k \geq 0$, and said address offset generating circuit is operable such that:

(i) if all of said high order field bits P_k have respective predetermined values D_k, then bits B_j of said N-bit address offset are given by $B_j = S$ for all values of j such that (N-1)≥j≥(N-L-1); and

(ii) if any of said high order field bits P_k does not have said predetermined value D_k, then bits B_j of said N-bit address offset, where (N-1)≥j≥(N-L-1), are given by a predetermined one-to-one mapping from combinations of values of said high order field bits P_k and said offset value sign specifying bit S to combinations of values of B_j other than the combination $B_j = 1$ for all values of j such that (N-1)≥j≥(N-L-1) and the combination $B_j = 0$ for all values of j such that (N-1)≥j≥(N-L-1).

13. A method as claimed in claim 12, wherein said predetermined values D_k are all equal to 1.

14. A method as claimed in claim 12, wherein said address offset generating circuit is operable to generate bit B_j values of said N-bit address offset each bit value B_j having a value given by a respective predetermined one of:

$B_j = S$ for one directly sign bit specified value of j;

$B_j = S \text{ XOR } P_{k(j)} \text{ XOR } D_{k(j)}$ where k(j) is a one-to-one index mapping from values of j, excluding said directly sign bit specified value of j, to values of k.

15. A method as claimed in claim 14, wherein said directly sign bit specified value of j is N-1.

16. A method as claimed in claim 12, wherein said address offset generating instruction is a branch instruction and said N-bit address offset is an N-bit branch target address offset.

17. A method as claimed in claim 16, wherein said N-bit branch target address offset is combined with a program address of said branch instruction to generate a branch target address.

18. A method as claimed in claim 12, wherein said N-bit address offset is further sign extended by said address offset generating instruction prior to use.

19. A method as claimed in claim 12, wherein $L = 2$.

20. A method as claimed in claim 12, wherein $N = 25$.

21. A method as claimed in claim 12, wherein Z is one of 1 and 2.

22. A method as claimed in claim 12, wherein bit values B_{N-2-L} to B_Z are directly specified in said address offset generating instruction.

23. A computer program product including a computer program for controlling a computer to perform the steps of:

controlling data processing operations using an instruction decoder responsive to program instructions; and

generating an N-bit address offset having a value specified by an address offset generating instruction including an offset value sign specifying bit S using an address offset generating circuit controlled by said instruction decoder; wherein

said N-bit address offset has bit values B_i when expressed as a two's complement number, where $(N-1) \geq i \geq Z$ and $(N-1) > Z \geq 0$, said address offset generating instruction includes L high order field bits P_k, where $(N-Z) > L \geq 1$ and $L > k \geq 0$, and said address offset generating circuit is operable such that:

(i) if all of said high order field bits P_k have respective predetermined values D_k, then bits B_j of said N-bit address offset are given by $B_j = S$ for all values of j such that $(N-1) \geq j \geq (N-L-1)$; and

(ii) if any of said high order field bits P_k does not have said predetermined value D_k, then bits B_j of said N-bit address offset, where $(N-1) \geq j \geq (N-L-1)$, are given by a predetermined one-to-one mapping from combinations of values of said high order field bits P_k and said offset value sign specifying bit S to combinations of values of B_j other than the combination $B_j = 1$ for all values of j such that $(N-1) \geq j \geq (N-L-1)$ and the combination $B_j = 0$ for all values of j such that $(N-1) \geq j \geq (N-L-1)$.

24. A computer program product as claimed in claim 23, wherein said predetermined values D_k are all equal to 1.

25. A computer program product as claimed in claim 23, wherein said address offset generating circuit is operable to generate bit B_j values of said N-bit address offset each bit value B_j having a value given by a respective predetermined one of:

$B_j = S$ for one directly sign bit specified value of j;

$B_j = S \text{ XOR } P_{k(j)} \text{ XOR } D_{k(j)}$ where k(j) is a one-to-one index mapping from values of j, excluding said directly sign bit specified value of j, to values of k.

26. A computer program product as claimed in claim 25, wherein said directly sign bit specified value of j is N-1.

27. A computer program product as claimed in claim 23, wherein said address offset generating instruction is a branch instruction and said N-bit address offset is an N-bit branch target address offset.

28. A computer program product as claimed in claim 27, wherein said N-bit branch target address offset is combined with a program address of said branch instruction to generate a branch target address.

29. A computer program product as claimed in claim 23, wherein said N-bit address offset is further sign extended by said address offset generating instruction prior to use.

30. A computer program product as claimed in claim 23, wherein L = 2.

31. A computer program product as claimed in claim 23, wherein N = 25.

32. A computer program product as claimed in claim 23, wherein Z is one of 1 and 2.

33. A computer program product as claimed in claim 23, wherein bit values B_{N-2-L} to B_Z are directly specified in said address offset generating instruction.